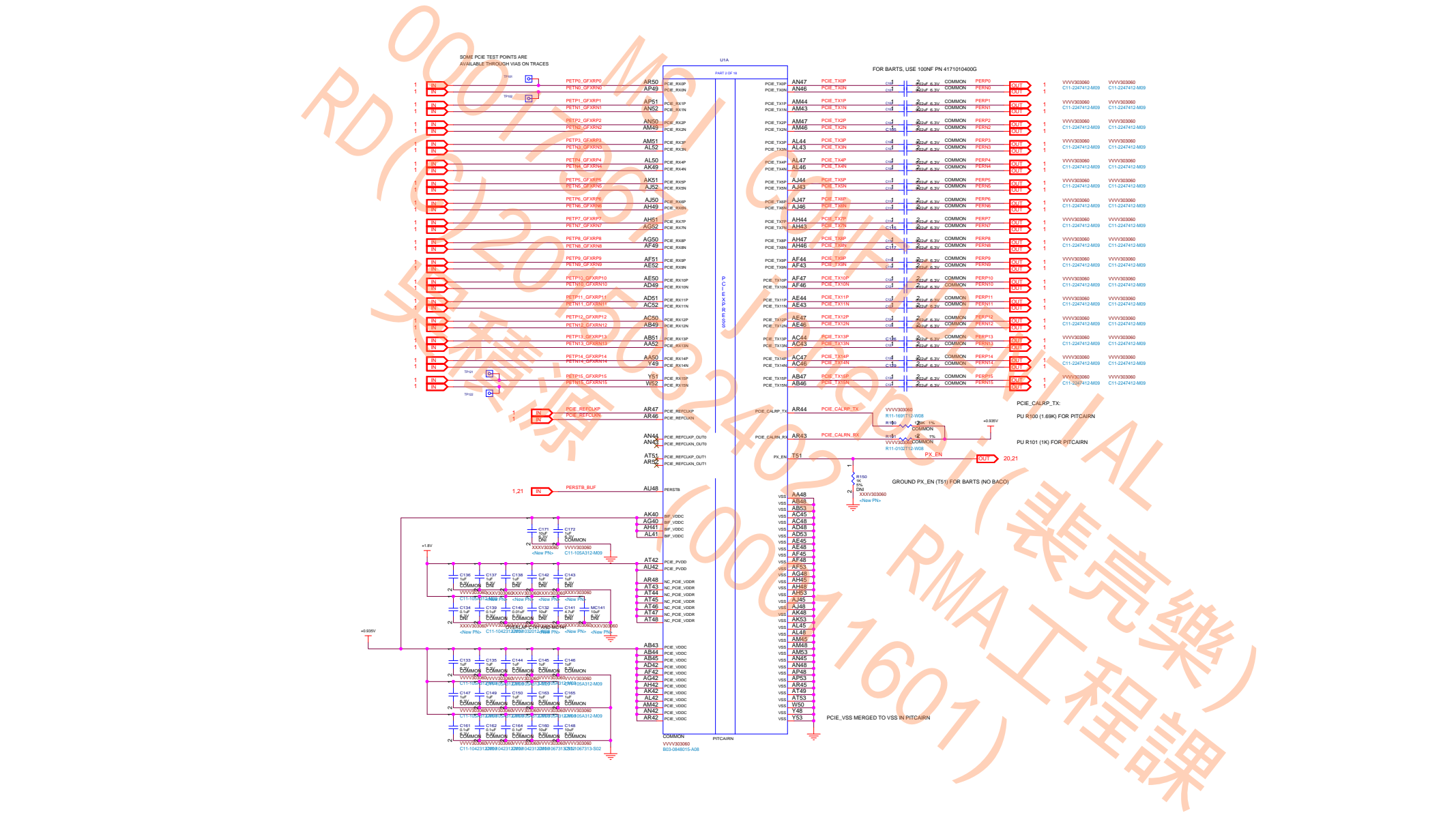
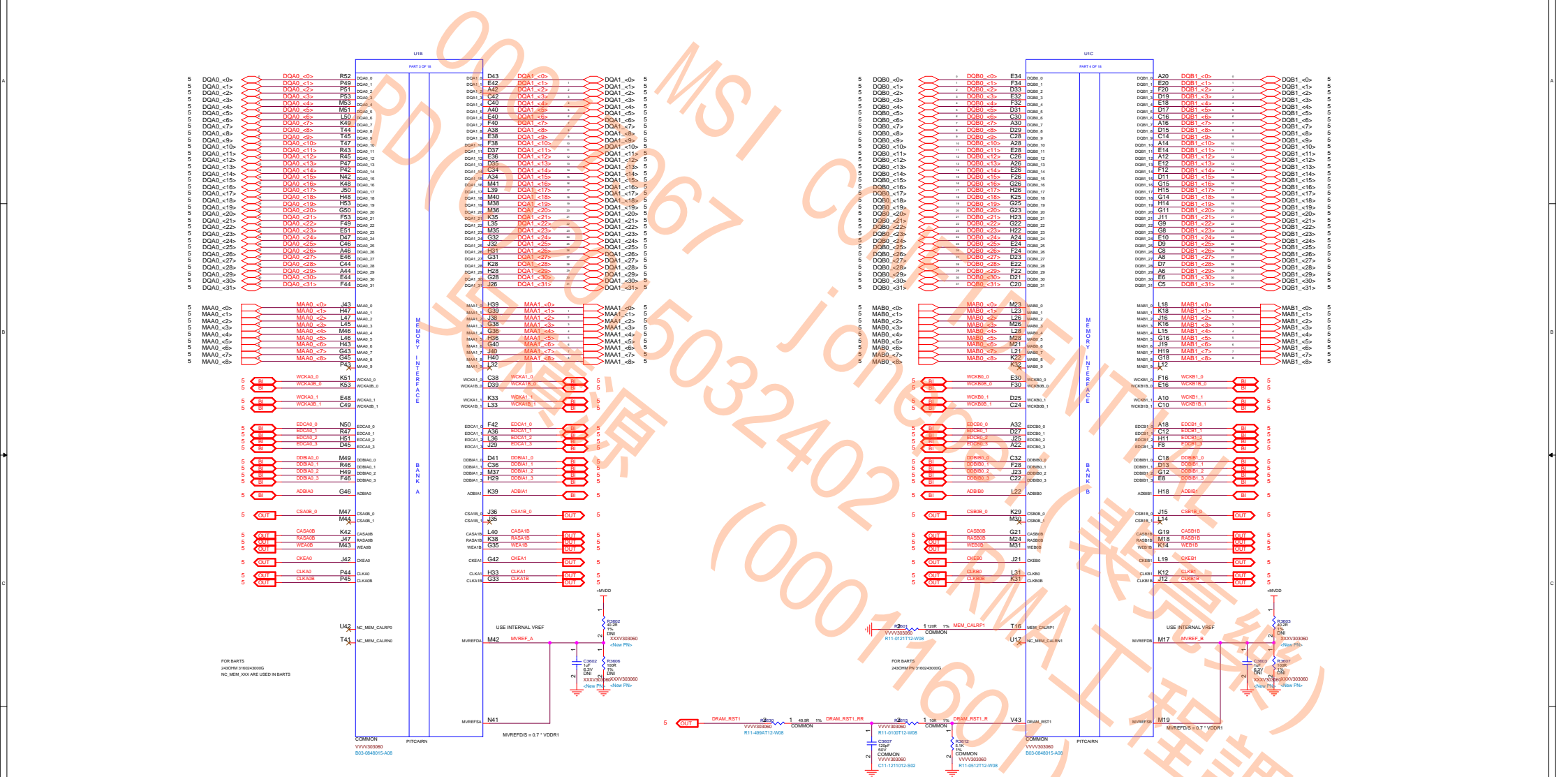


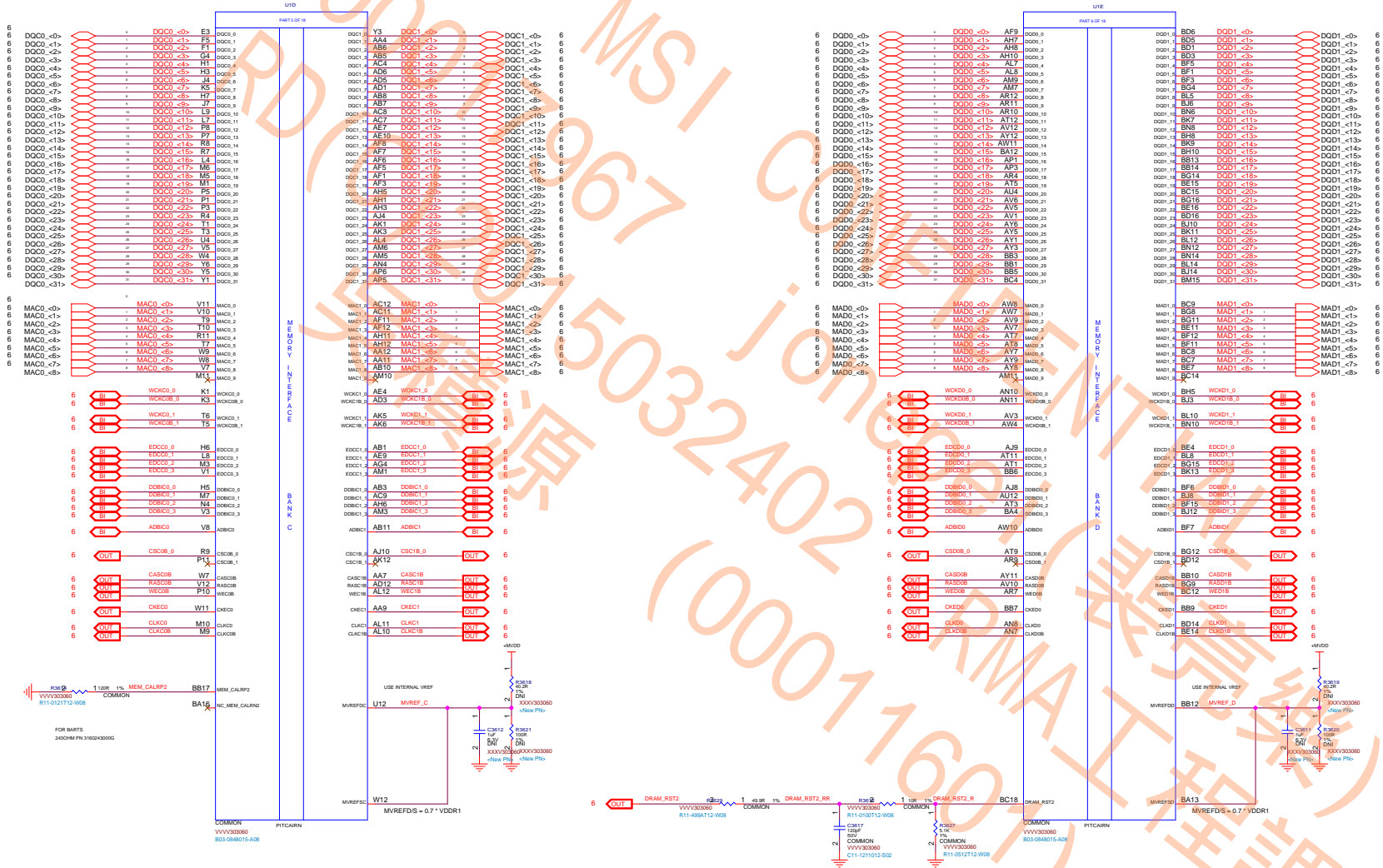
(2) CURACAO PCIE INTERFACE



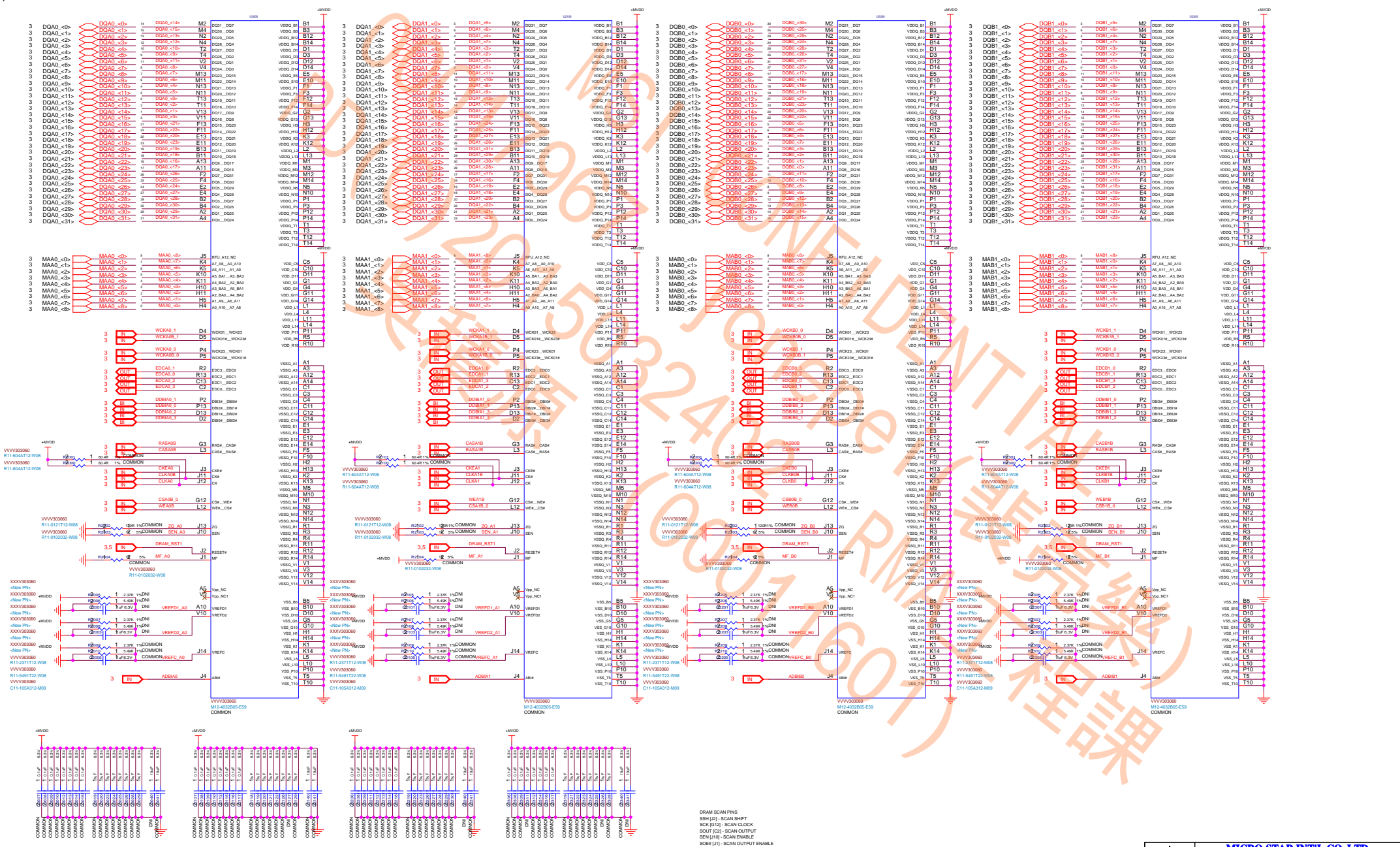
(3) CURACAO MEM INTERFACE CH AB



(4) CURACAO MEM INTERFACE CH CD

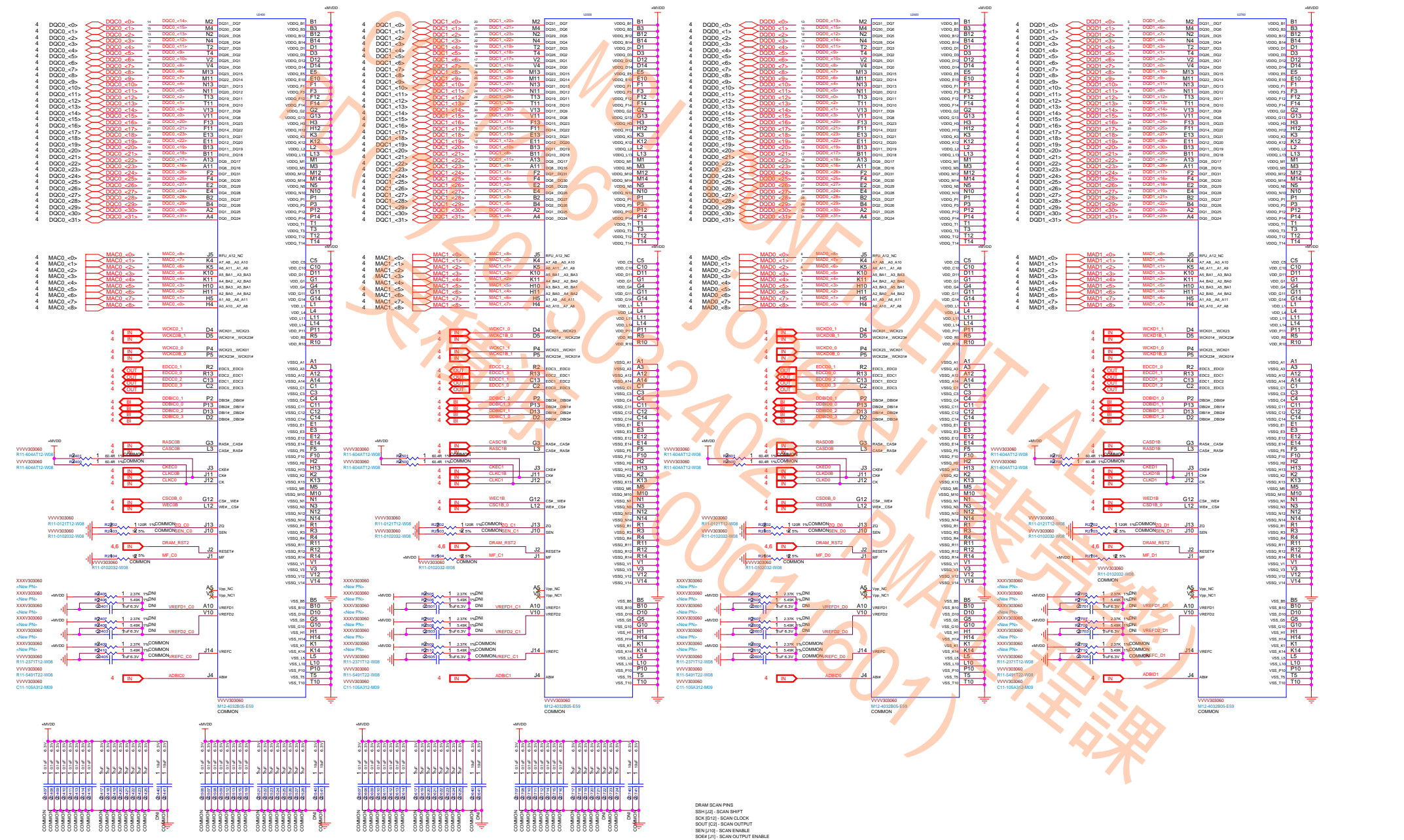


(5) GDDR5 MEM CH AB

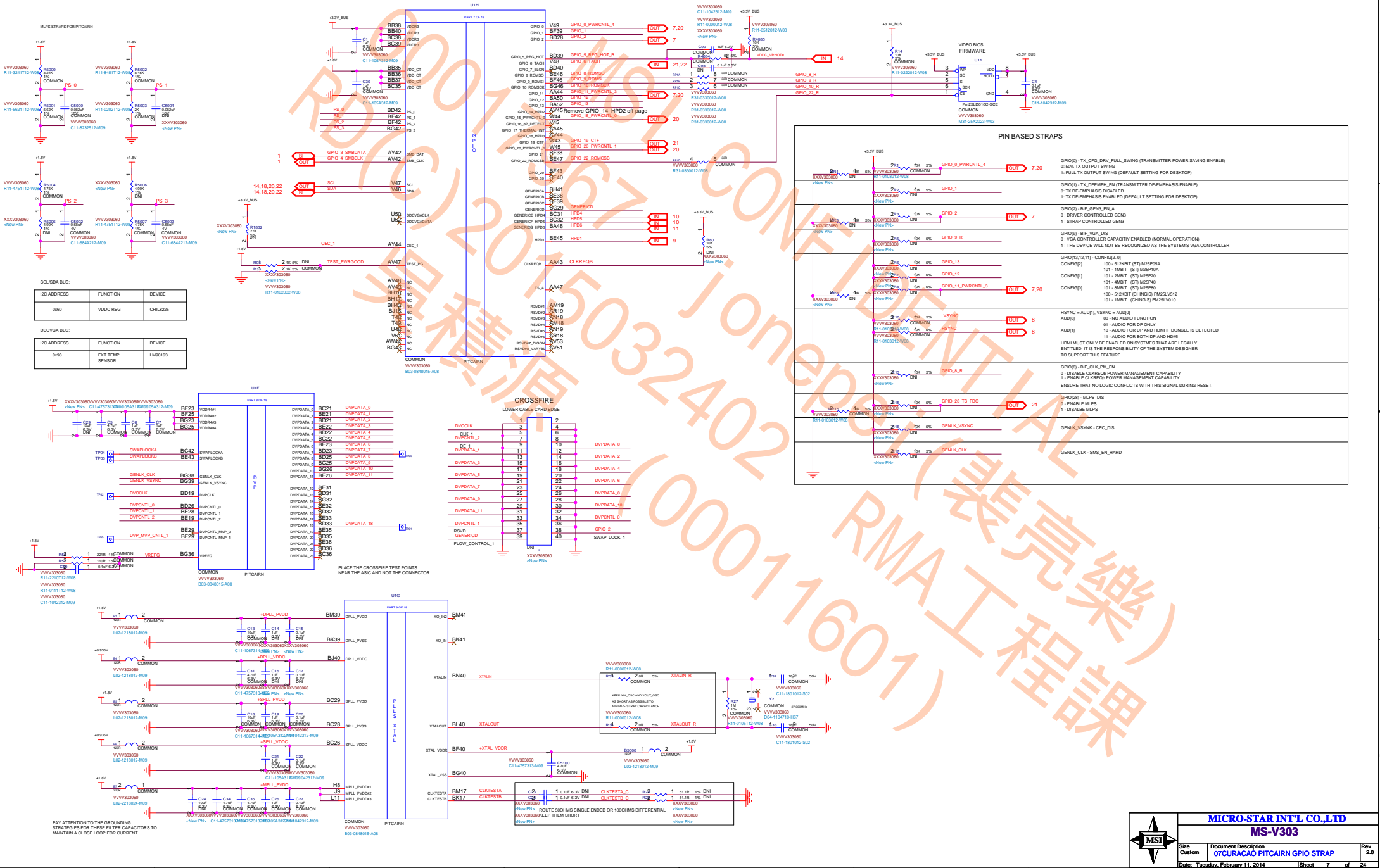


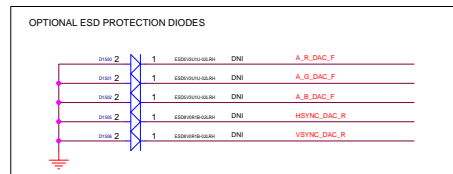


(6) GDDR5 MEM CH CD

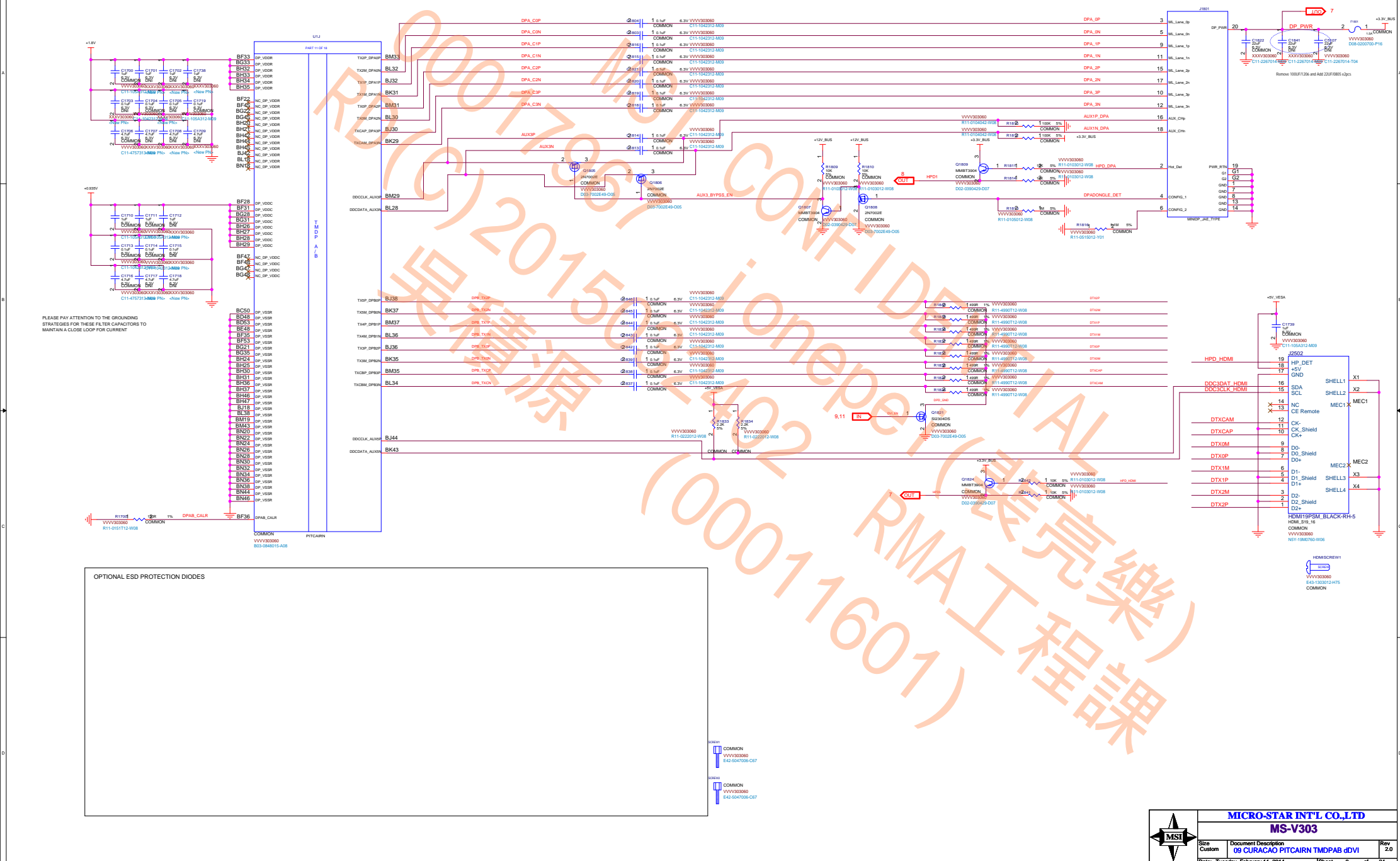


(7) CURACAO GPIO STRAP CF PLL XTAL



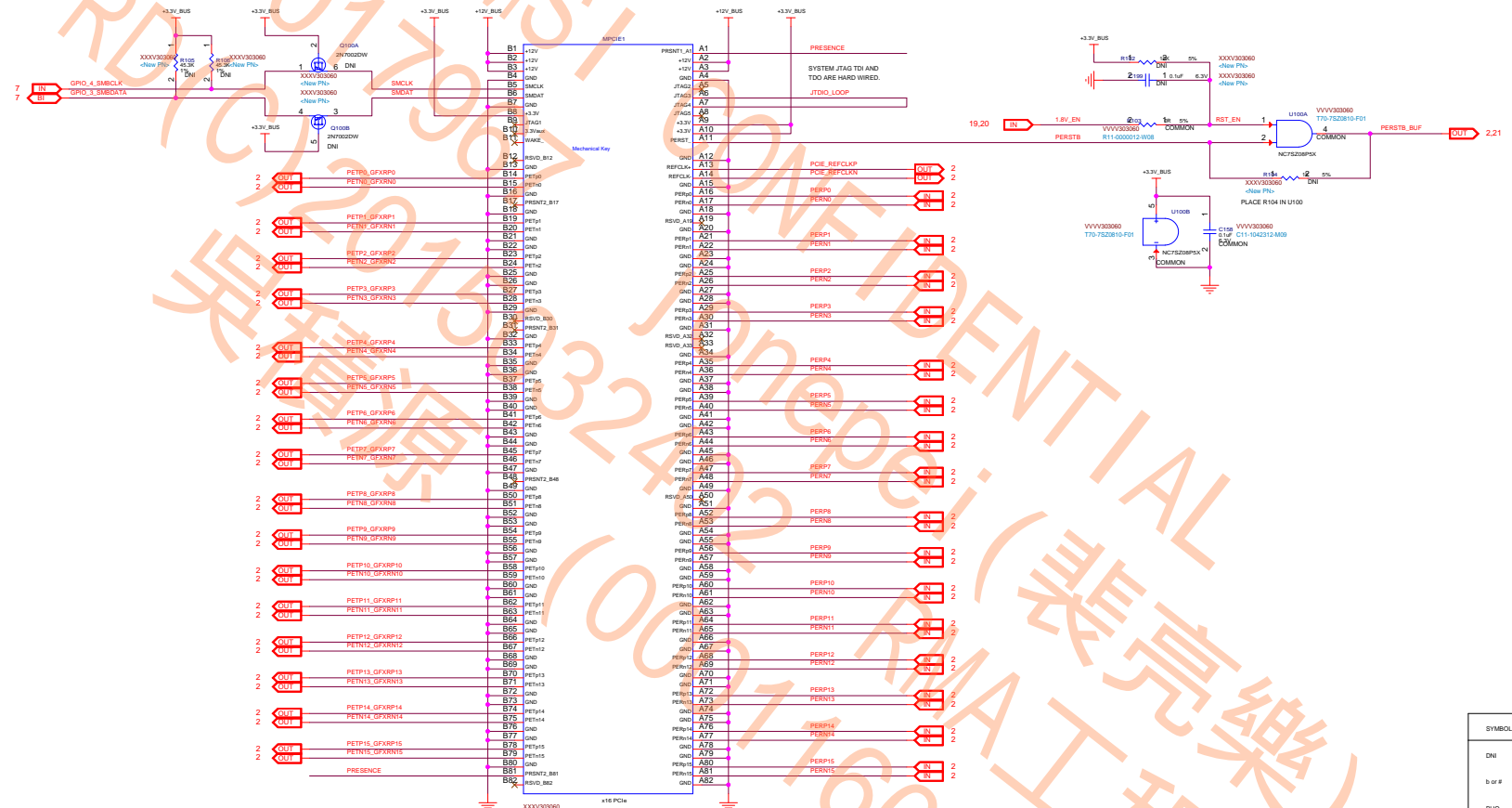
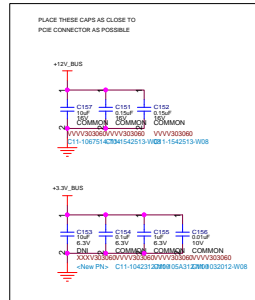




(9) CURACAO TMDPAB sDVI





(1) PCI-EXPRESS EDGE CONNECTOR



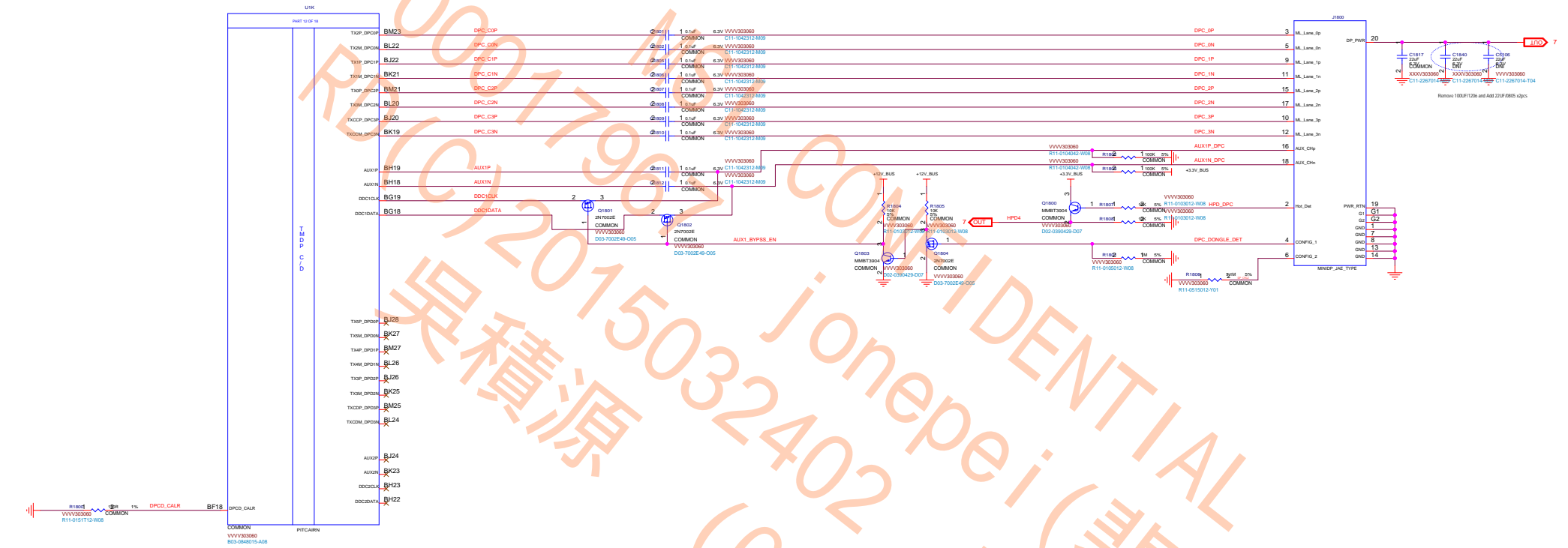
SYMBOL LEGEND	
DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

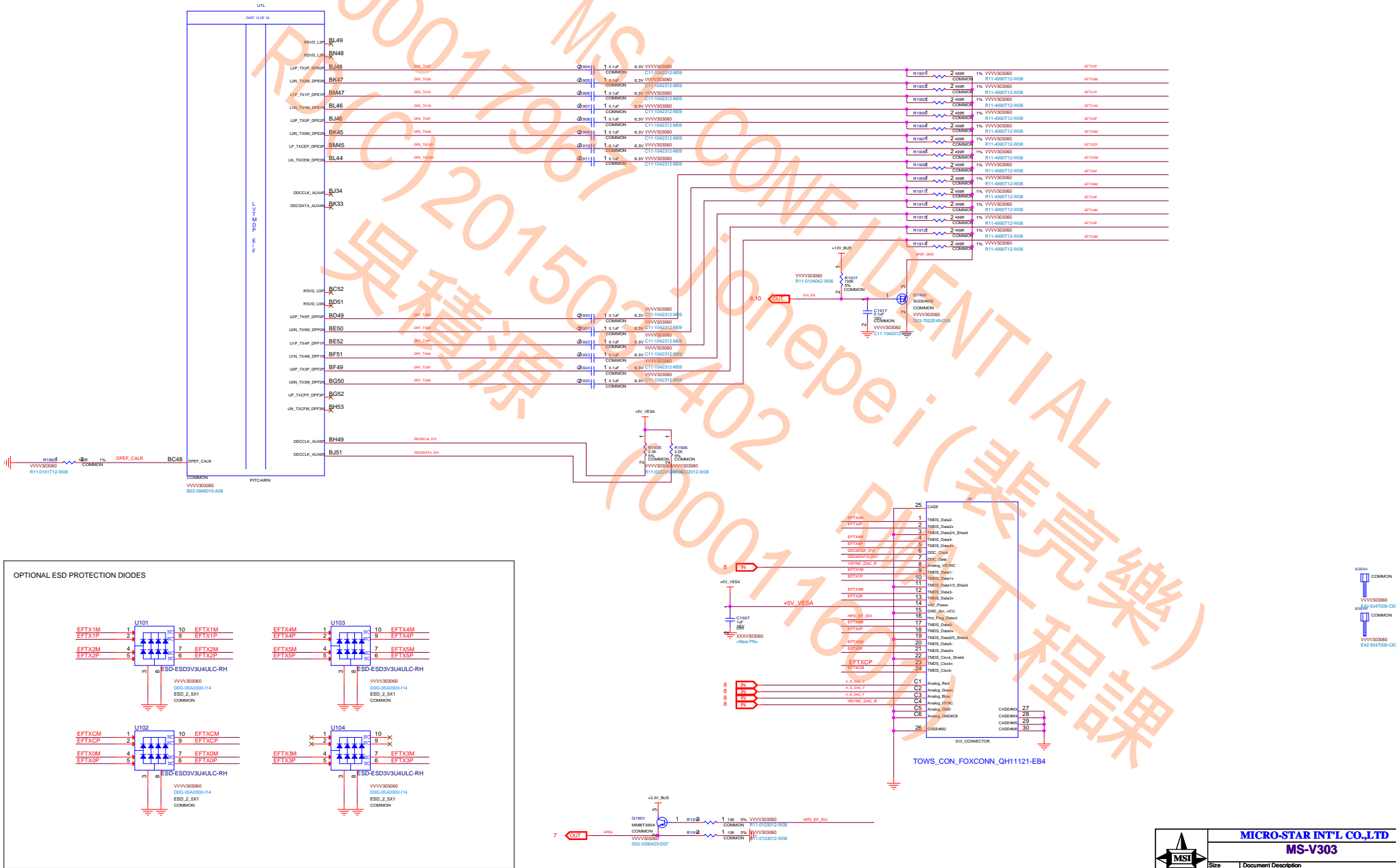


**MICRO-STAR INT'L CO.,LTD**

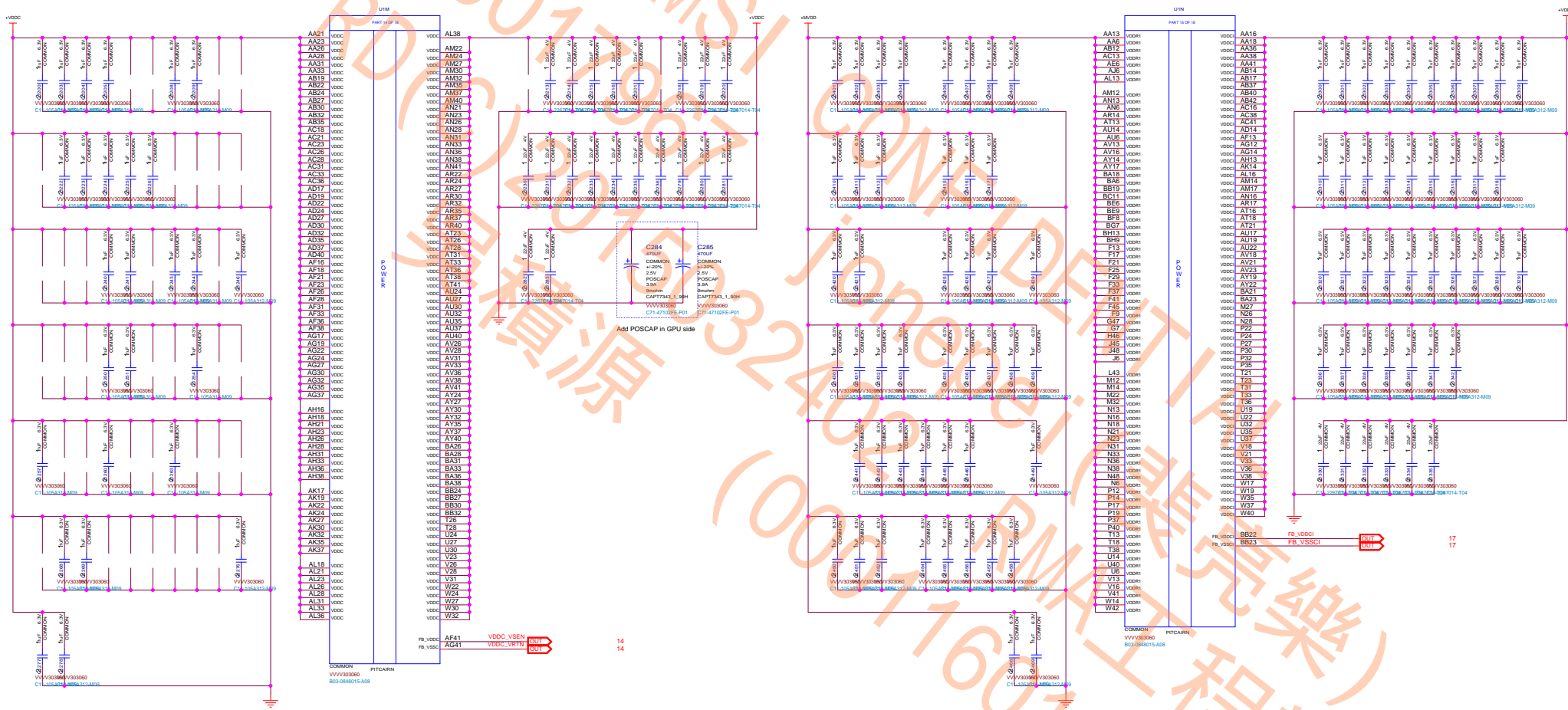
MS-V303

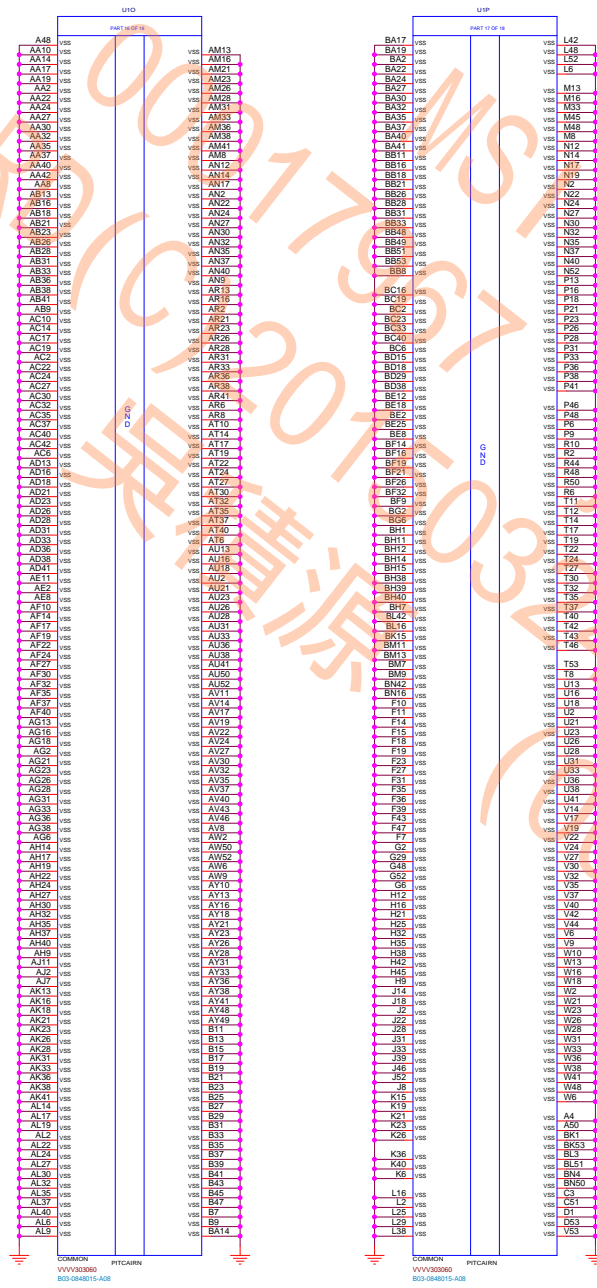
Size Custom	Document Description <b>01 PCIE EDGE CONNECTOR</b>	Rev 2.0
Date: Tuesday, February 11, 2014		Sheet 1 of 24



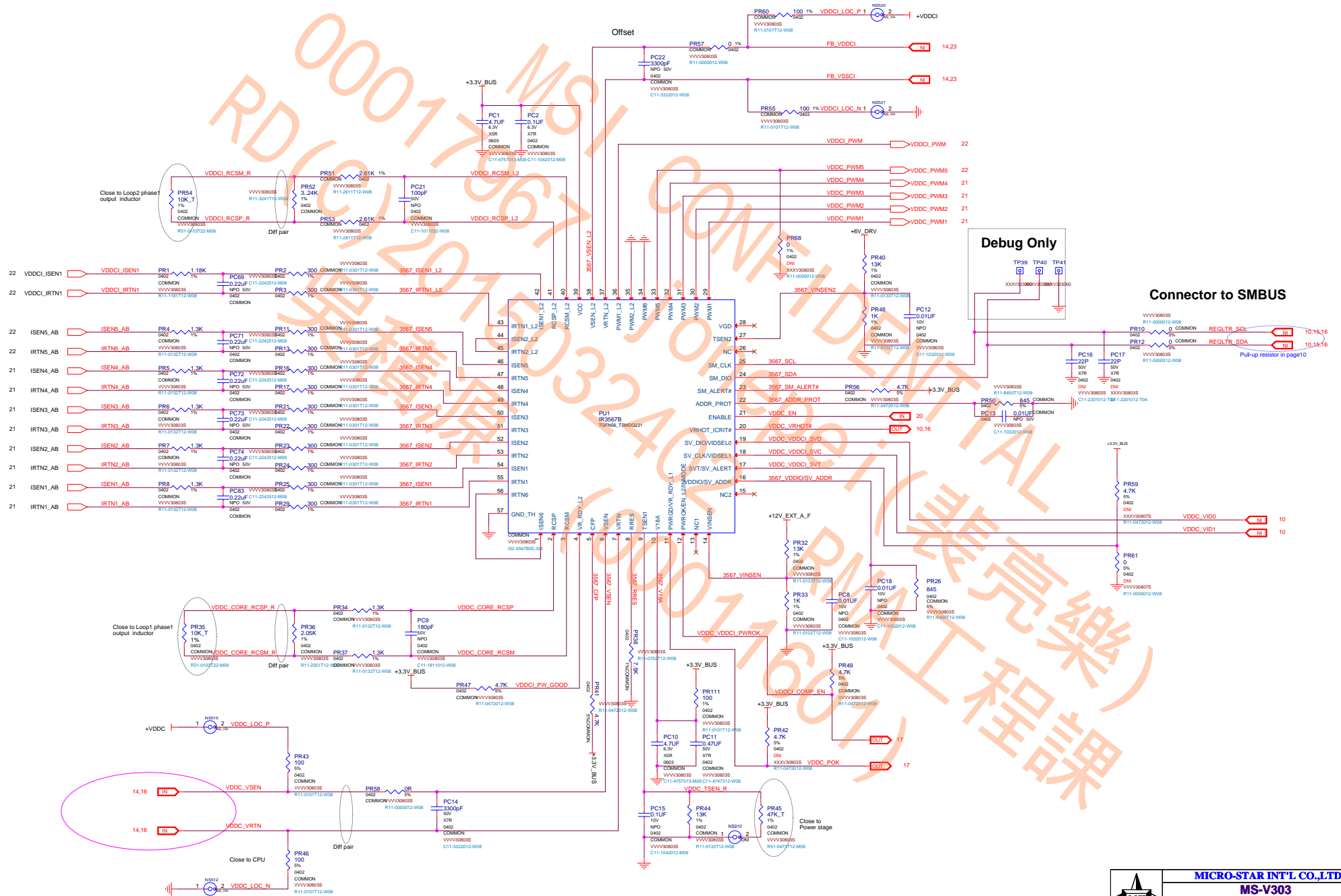


(12) CURACAO POWER

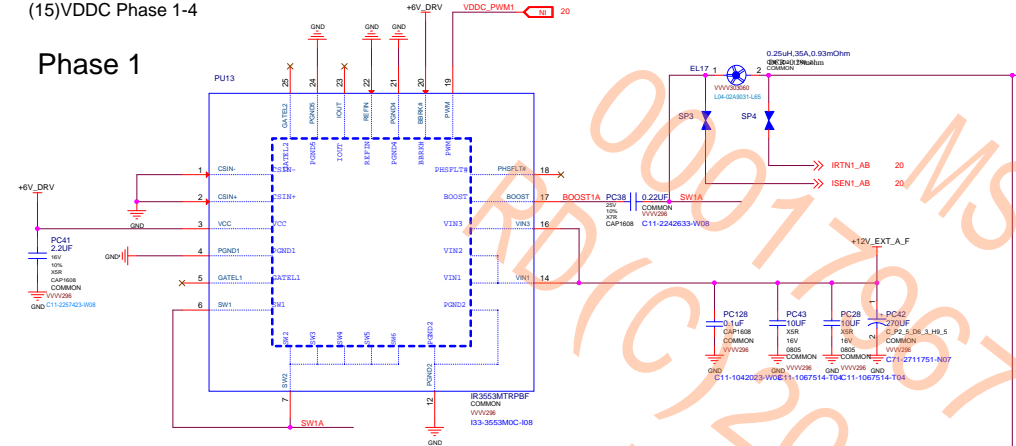




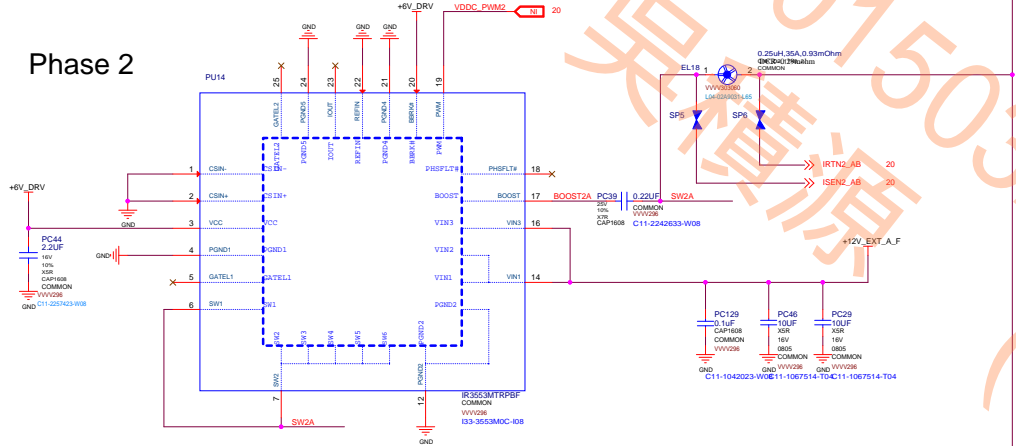




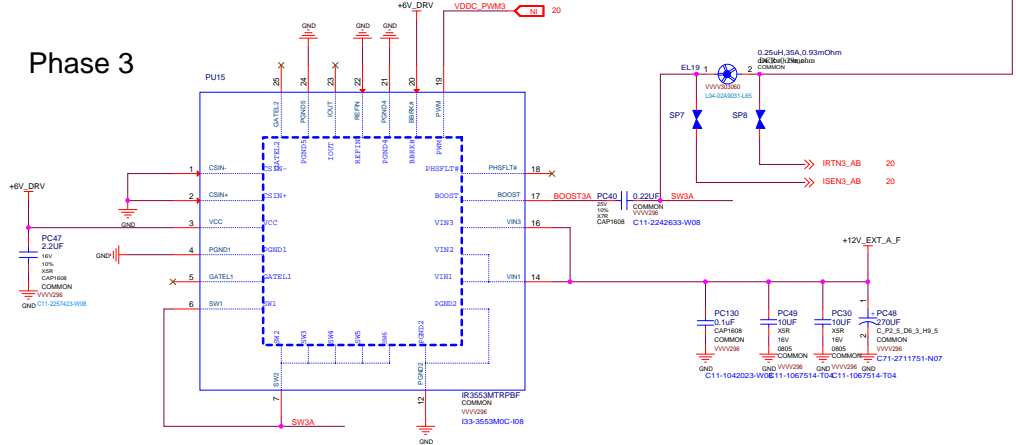
Phase 1



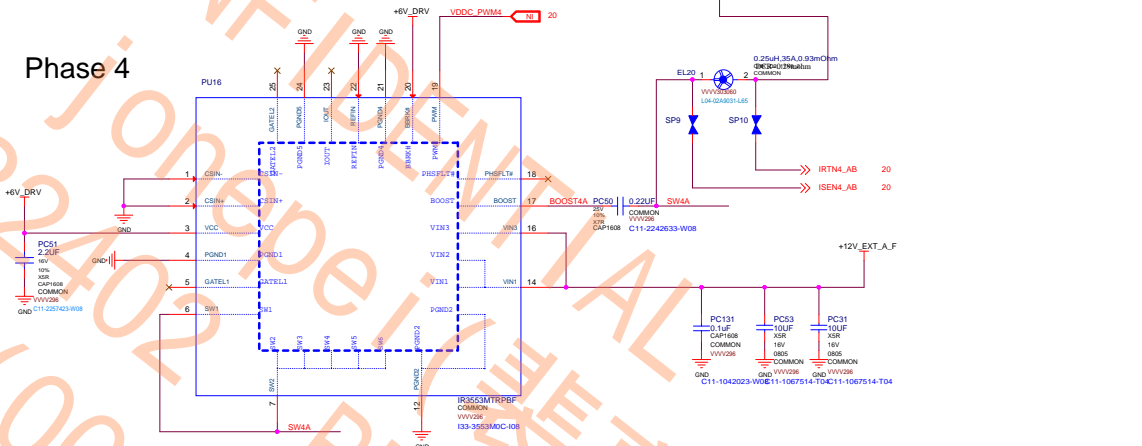
Phase 2



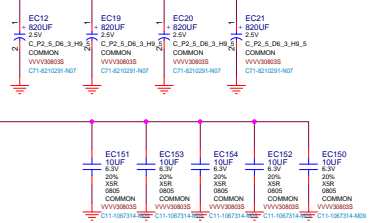
Phase 3

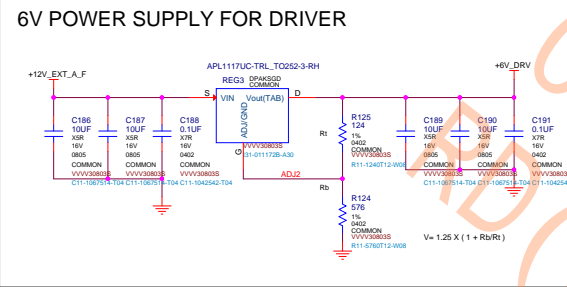


Phase 4

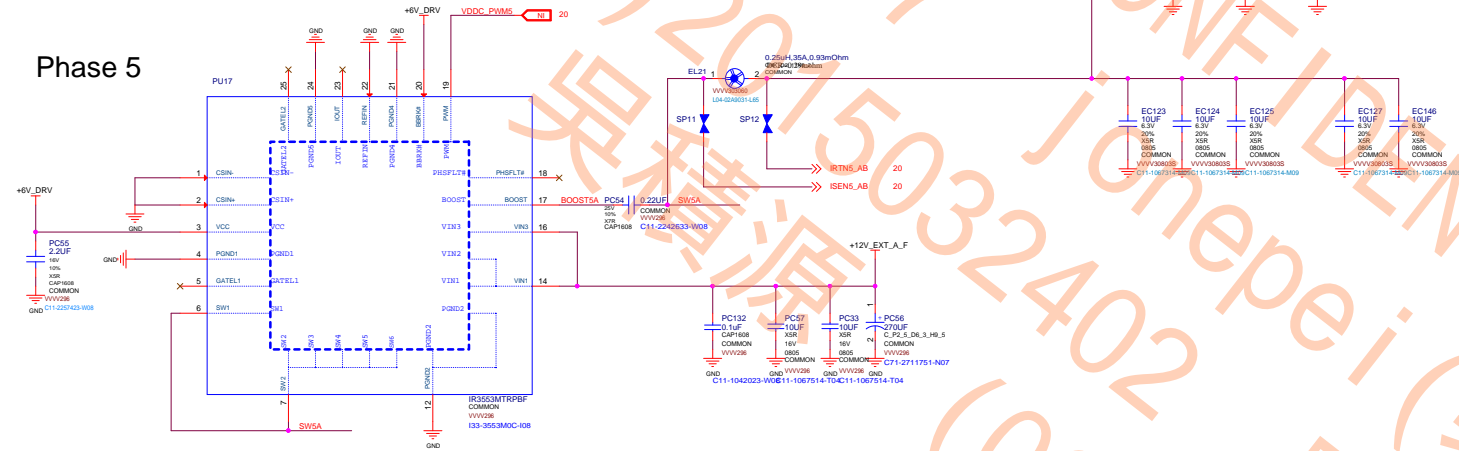


Output Bulk CAPs

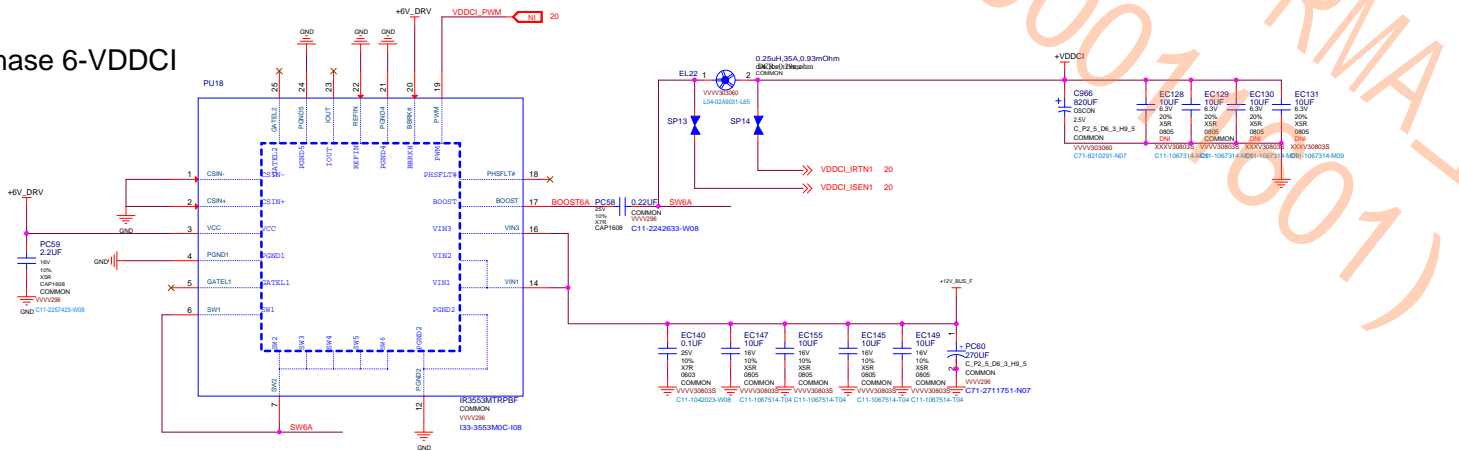




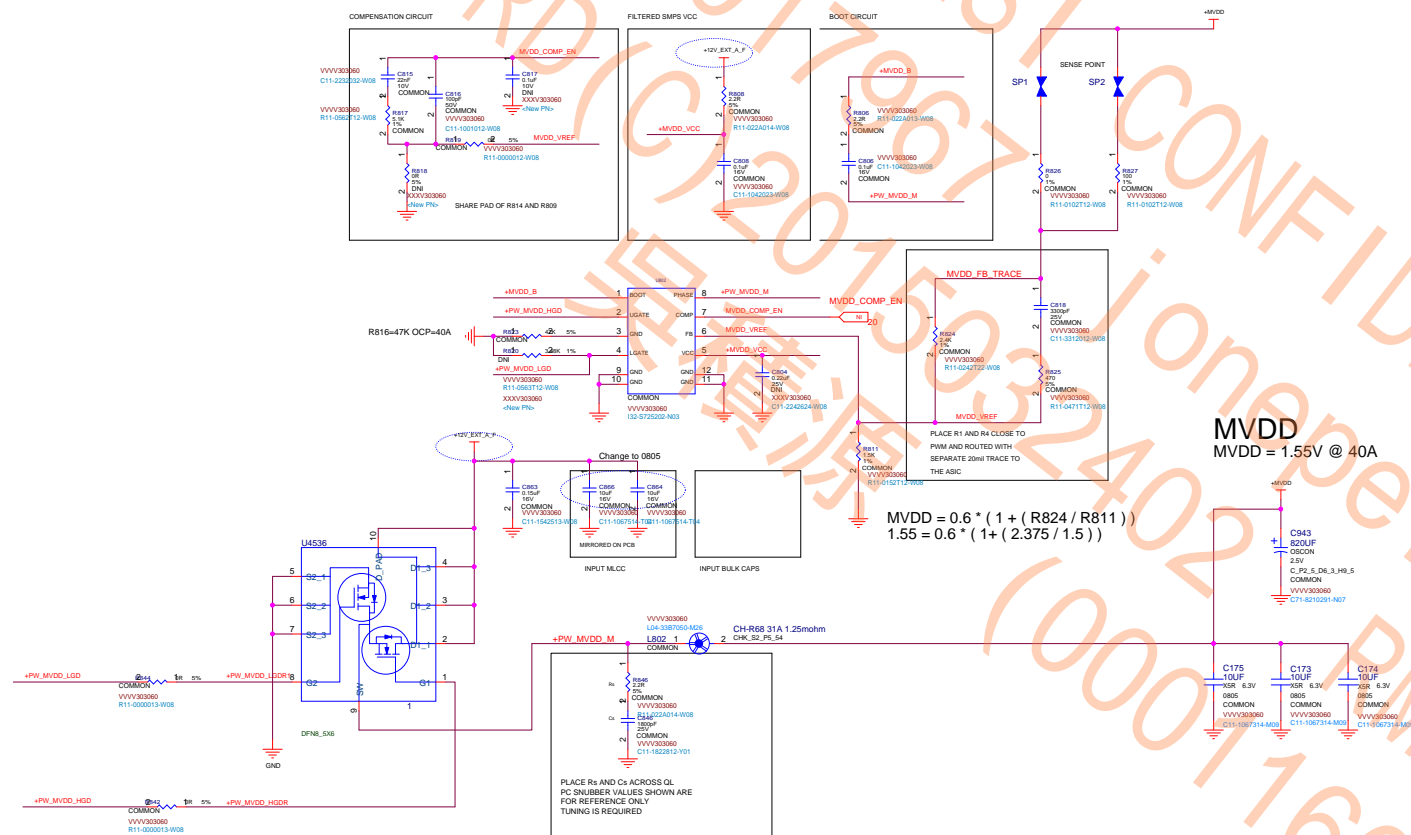
Phase 5



Phase 6-VDDCI



MSI CONFIDENTIAL  
00017967 jonepei (裴亮樂)  
RD(C)2015032402 RMA工程課  
吳積源 (00011601)

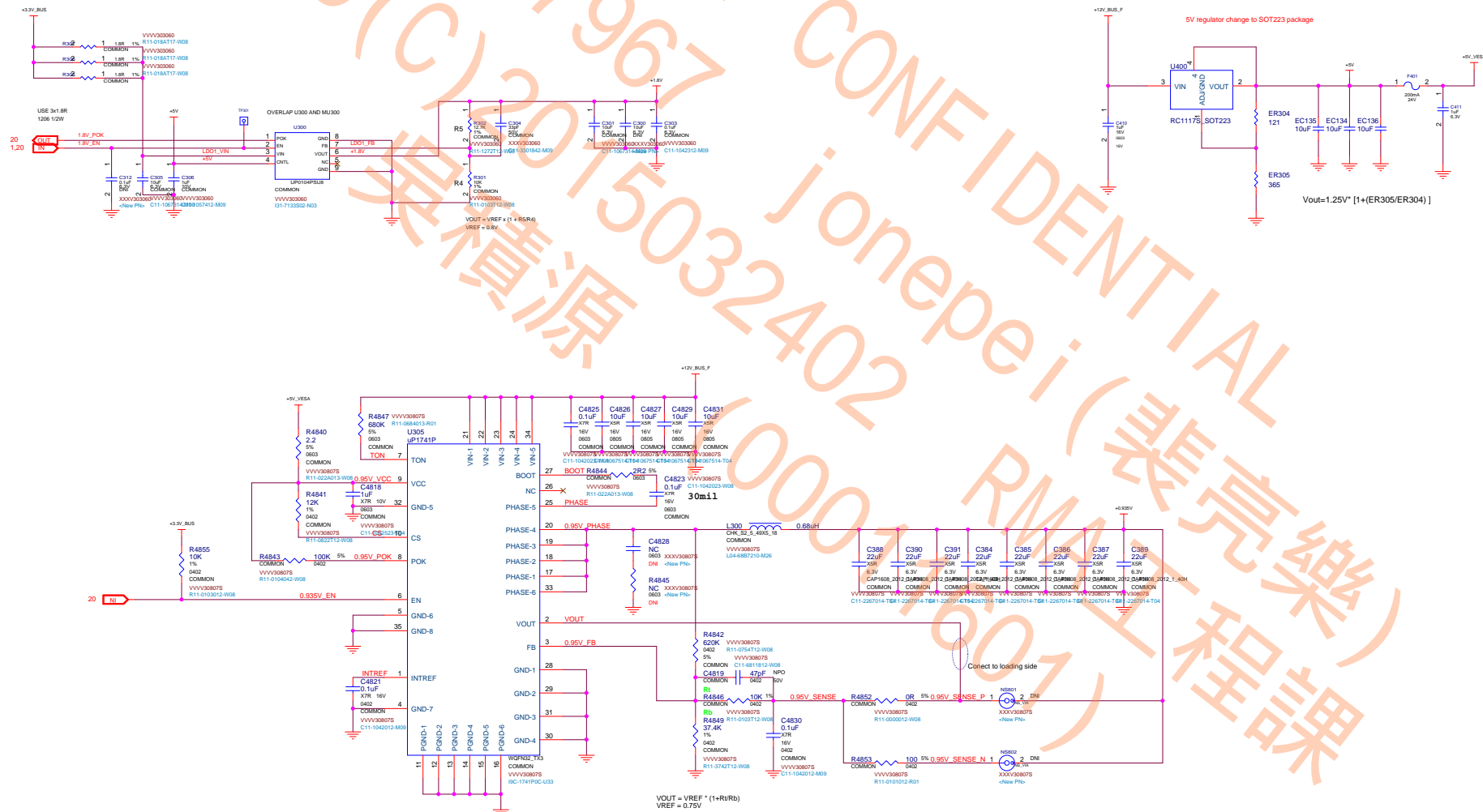




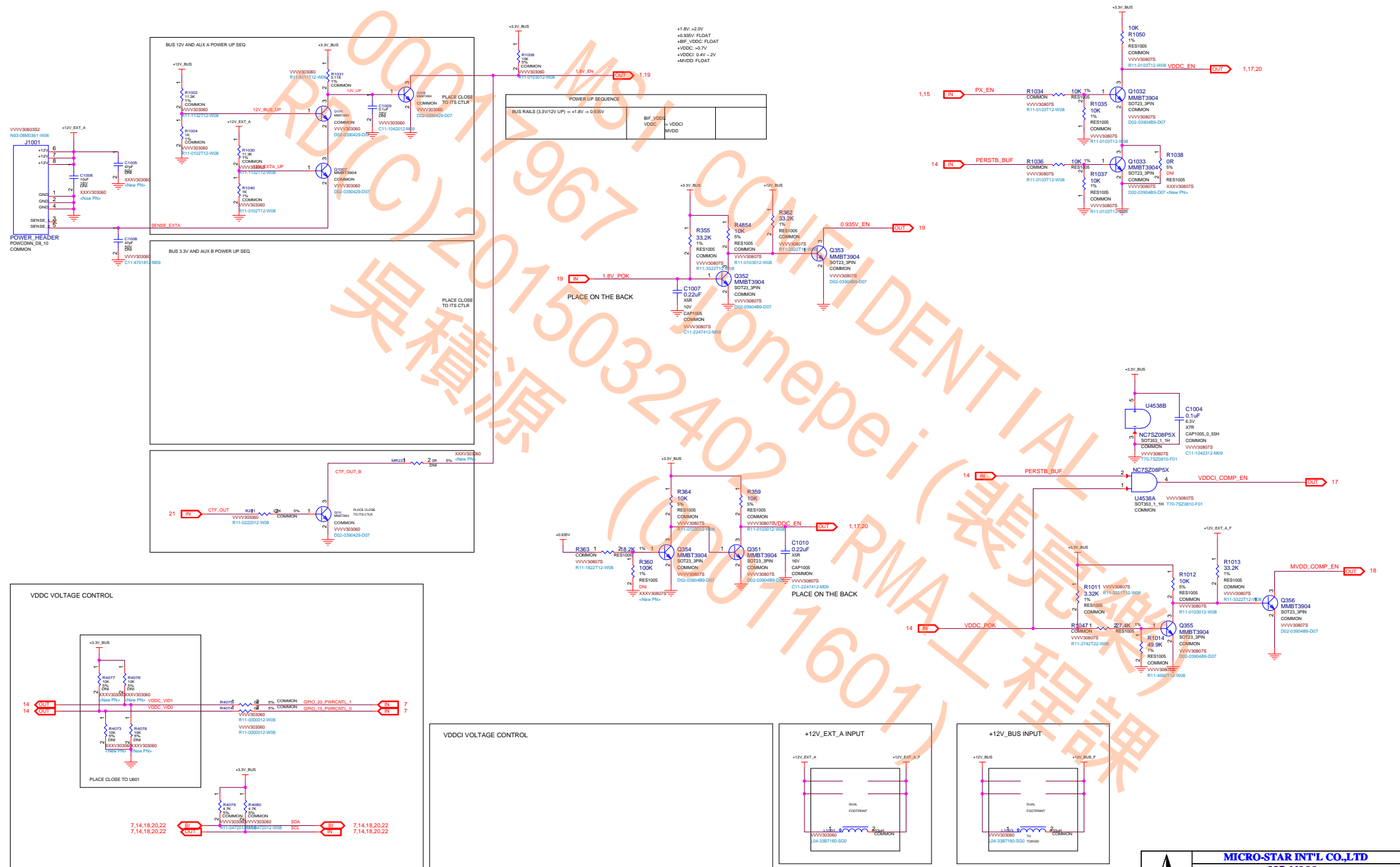
(18) SMALL RAIL REGULATOR

LDO #1: VIN = 3.0V TO 3.6V MAX      VOUT = +1.8V +/- 2%      IOUT = 1.3A RMS MAX  
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

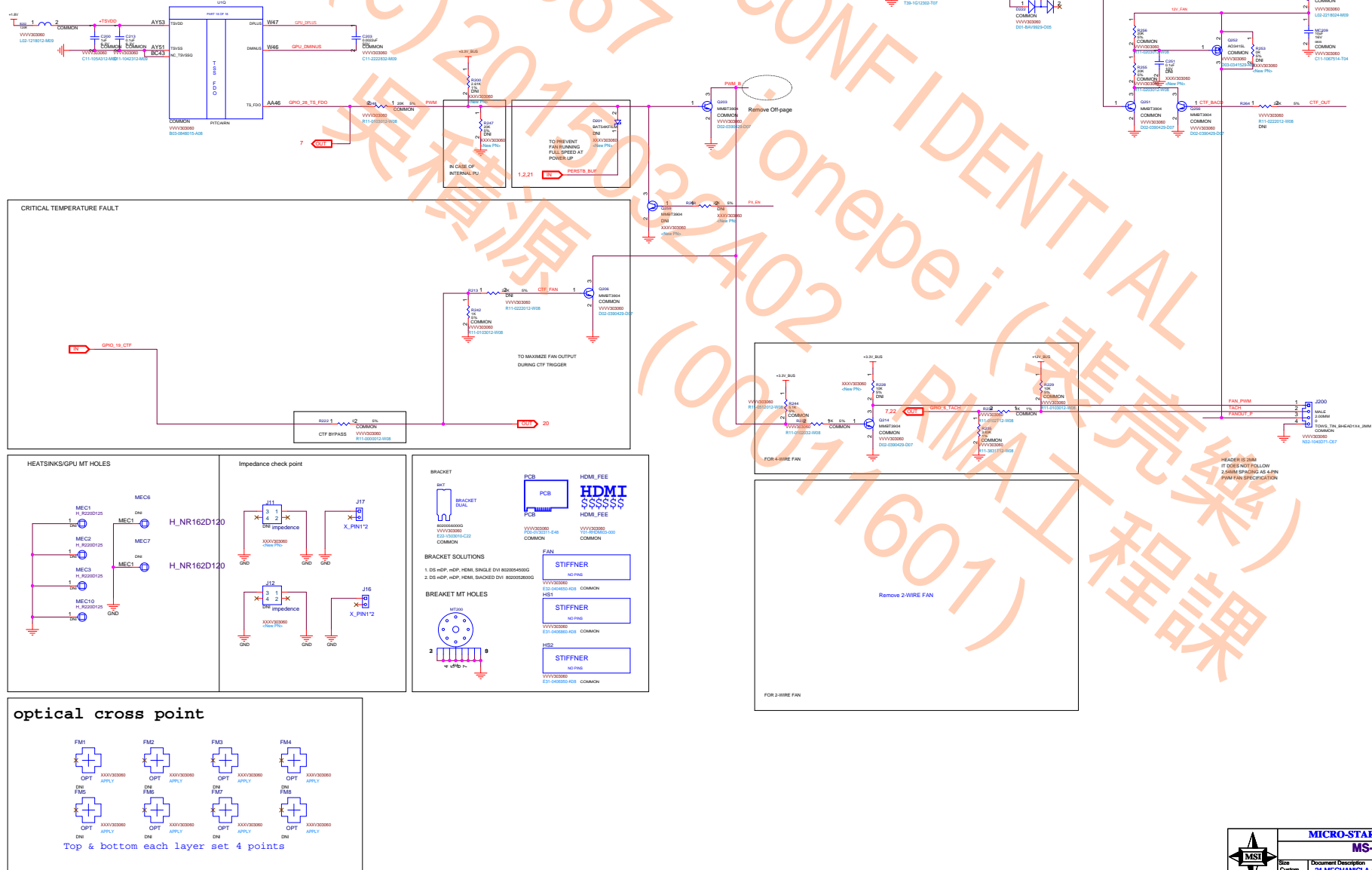
REGULATOR FOR +5V RAILS  
IOUT MAX = 150mA



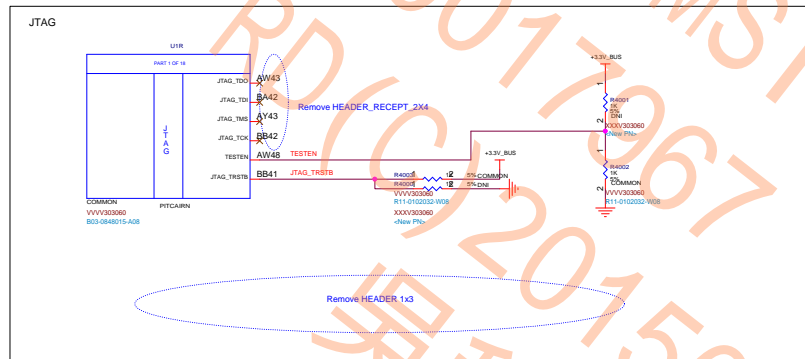
(19) POWER MANAGEMENT



(20) MECH AND THERM MANAGEMENT



(21) DEBUG CIRCUIT



### SWITCH CONNECTIONS TO PINSTRAPS

Remove

## LED LIGHTS

Remove

### V-Check Point

LM96163 FOR BACKUP THERMAL CONTROL

Remove

## I2C ACCESS POINTS FOR VDDC CONTROLLER

Remove

Remove

Thermal IC





0	00A	12/07/2012	INITIAL SCHEMATIC BASED ON C400
1	00B	30/10/2012	add R688,C98,C99
1	00C	25/12/2012	remove L1720 ~ L1733 remove NC pin for DP_VDDR/DP_VDDC
	00D	19/06/2013	update power sequence to make 0.95V power up before vddc
V303-1.0	01/08/2013	Page07 : Remove GPIO_14_HPD2 off-page Add Dual-BIOS & Switch Page10 : Change J2501 footprint and Library Page11 : Add optional ESD Protection DIODES Page12 : Add C284/C285 (POSCAP) Remove some 1UF/0402 of VDDC Page14 : Change VDDC controller to 8228G Page15 : Add Driver IR3598 circuit Page16 : Add Driver IR3598 circuit Page17 : Change L801 footprint Change VDDCI_VIN Page18 : Page14 : Change MVDD controller to uP1610PQAG Page19 : Change +5V circuit Change 0.935V_VCC to +12V_BUS_F Page20 : Add R7341/R7342/L1506 Del R1090~R1095 Page21 : Remove 2-wire FAN circuit Page22 : Remove JTAG pin header Remove SWITCH CONNECTIONS TO PINSTRAPS Remove LED LIGHTS Remove I2C ACCESS POINTS FOR VDDC CONTROLLER Add V-Check Point and Thermal IC	
V303-1.1	06/08/2013	Page14 : Controller change to IR3563B	
V303-2.0	01/23/2014	Page07 : Remove OSC & dual vbios circuit Page09 : DPA chahge to mDP DPB chahge to HDMI Page10 : DPC chahge to mDP Page14 : change to IR3567 , reference V308-2.0 Page15 : change MOS , reference V296-1.1 Page16 : change MOS , reference V296-1.1 Page18 : MVDD reference V303-1.1 VDDCI circuit Page19 : remove MU300 & +0.935V used Regulator , +5V change to TO223 Page20 : POWER sequence reference V308-2.2 Page21 : remove CTF Page22 : remove DEBUG CIRCUIT	